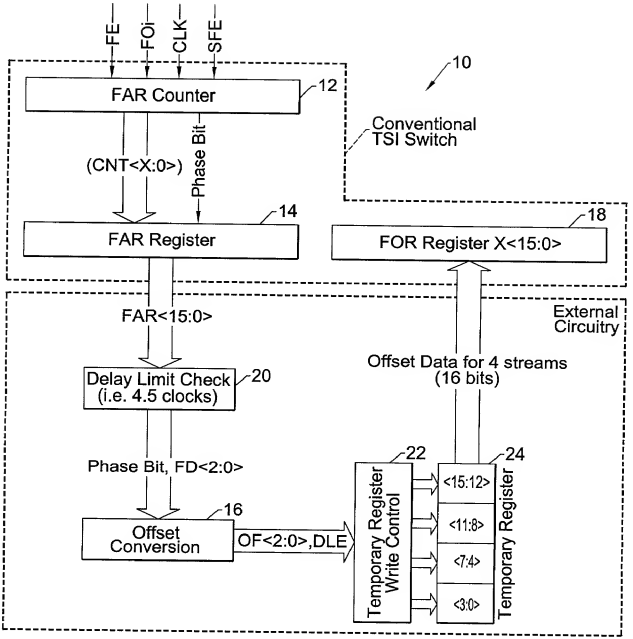

FIG. 1.
(PRIOR ART)

Input Stream Offset	Measurement Result from Frame Delay Bits				Corresponding Offset Bits			
	FD11	FD2	FD1	FD0	OFn2	OFn1	OFn0	DLEn
No clock period shift (Default)	1	0	0	0	0	0	0	0
+0.5 clock period shift	0	0	0	0	0	0	0	1
+1.0 clock period shift	1	0	0	1	0	0	1	0
+1.5 clock period shift	0	0	0	1	0	0	1	1
+2.0 clock period shift	1	0	1	0	0	1	0	0
+2.5 clock period shift	0	0	1	0	0	1	0	1
+3.0 clock period shift	1	0	1	1	0	1	1	0
+3.5 clock period shift	0	0	1	1	0	1	1	1
+4.0 clock period shift	1	1	0	0	1	0	0	0
+4.5 clock period shift (max)	0	1	0	0	1	0	0	1

FIG. 2.
(PRIOR ART)

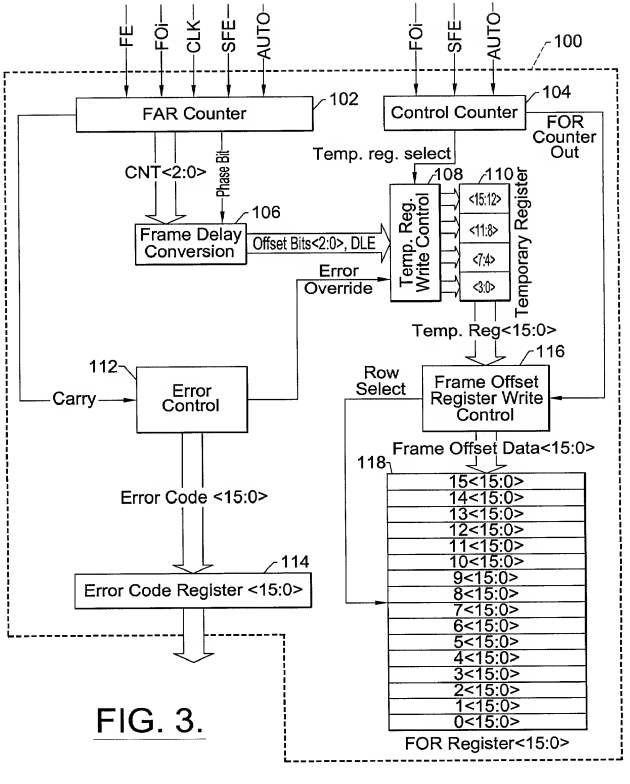
FE
FOi
CLK
SFE
AUTO
FOi
SFE
AUTO
100
FAR Counter
102
Control Counter
104
FOR Counter Out
Temp. reg. select
CNT<2:0>
Phase Bit
108
110
106
Frame Delay Conversion
Offset Bits<2:0>, DLE
Temp. Reg. Write Control
<15:12>
<11:8>
<7:4>
<3:0>
Temporary Register
Error Override
Temp. Reg<15:0>
112
Carry
Error Control
Row Select
116
Frame Offset Register Write Control
Frame Offset Data<15:0>
118
Error Code <15:0>
15<15:0>
14<15:0>
13<15:0>
12<15:0>
11<15:0>
10<15:0>
9<15:0>
8<15:0>
7<15:0>
6<15:0>
5<15:0>
4<15:0>
3<15:0>
2<15:0>
1<15:0>
0<15:0>
114
Error Code Register <15:0>
FOR Register<15:0>

FIG. 3.

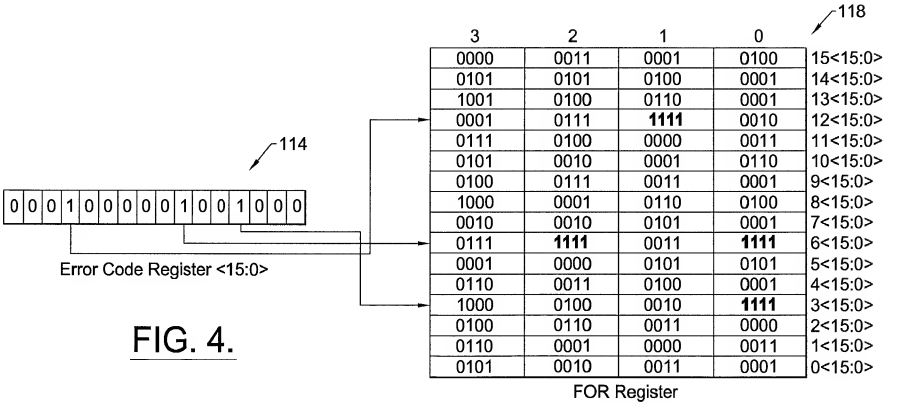

FIG. 4.

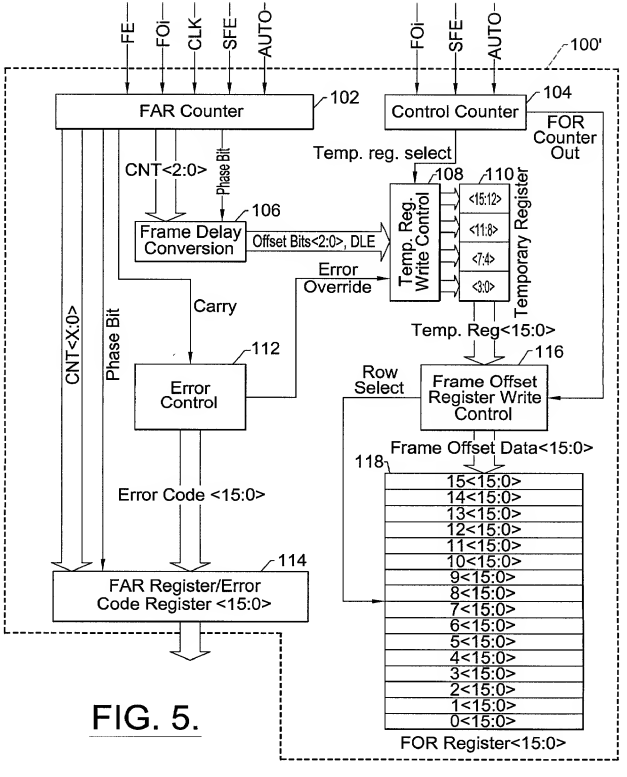
FE
FOI
CLK
SFE
AUTO
FOI
SFE
AUTO
100'
FAR Counter
102
Control Counter
104
FOR Counter Out
Temp. reg. select
CNT<2:0>
Phase Bit
108
110
106
Frame Delay Conversion
Offset Bits<2:0>, DLE
Temp. Reg. Write Control
<15:12>
<11:8>
<7:4>
<3:0>
Temporary Register
Error Override
Carry
CNT<X:0>
Phase Bit
Temp. Reg<15:0>
112
116
Row Select
Error Control
Frame Offset Register Write Control
Frame Offset Data<15:0>
118
Error Code <15:0>
15<15:0>
14<15:0>
13<15:0>
12<15:0>
11<15:0>
10<15:0>
9<15:0>
8<15:0>
7<15:0>
6<15:0>
5<15:0>
4<15:0>
3<15:0>
2<15:0>
1<15:0>
0<15:0>
114
FAR Register/Error Code Register <15:0>
FOR Register<15:0>

FIG. 5.

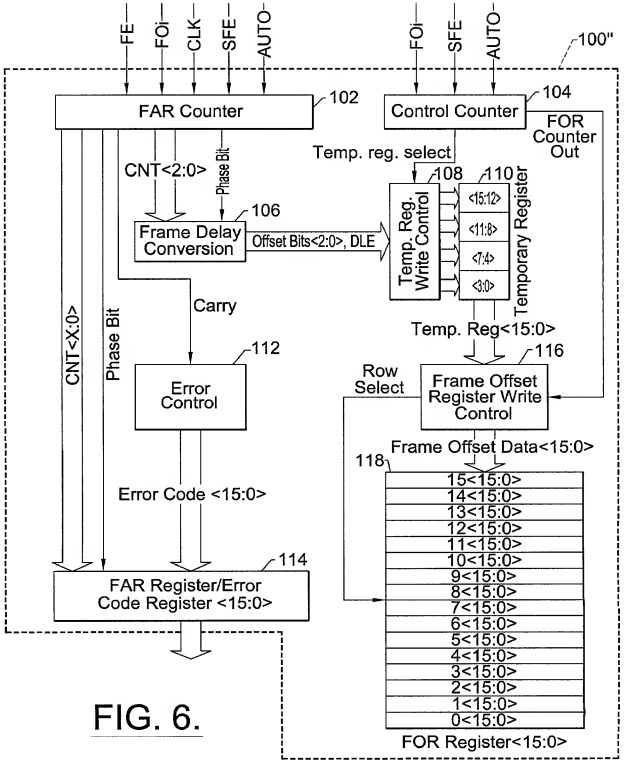
FE
FOi
CLK
SFE
AUTO
FOi
SFE
AUTO
100"
FAR Counter
102
Control Counter
104
FOR Counter Out
Temp. reg. select
CNT<2:0>
Phase Bit
108
110
106
Frame Delay Conversion
Offset Bits<2:0>, DLE
Temp. Reg. Write Control
<15:12>
<11:8>
<7:4>
<3:0>
Temporary Register
Carry
CNT<X:0>
Phase Bit
Temp. Reg<15:0>
112
116
Row Select
Error Control
Frame Offset Register Write Control
Frame Offset Data<15:0>
118
Error Code <15:0>
15<15:0>
14<15:0>
13<15:0>
12<15:0>
11<15:0>
10<15:0>
9<15:0>
8<15:0>
7<15:0>
6<15:0>
5<15:0>
4<15:0>
3<15:0>
2<15:0>
1<15:0>
0<15:0>
114
FAR Register/Error Code Register <15:0>
FOR Register<15:0>

FIG. 6.

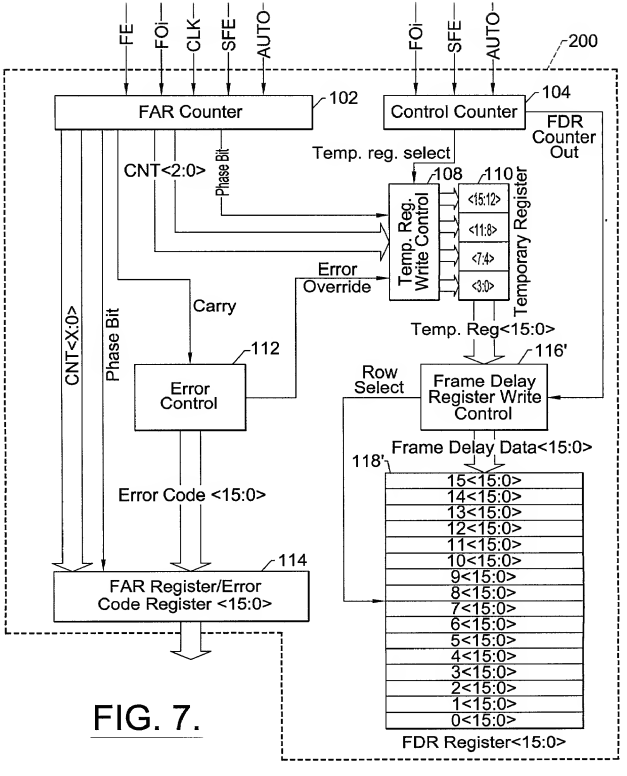
FE
FOI
CLK
SFE
AUTO
FOI
SFE
AUTO
200
FAR Counter
102
Control Counter
104
FDR Counter Out
Temp. reg. select
CNT<2:0>
Phase Bit
108
110
Temp. Reg. Write Control
<15:12>
<11:8>
<7:4>
<3:0>
Temporary Register
Error Override
Carry
CNT<X:0>
Phase Bit
Temp. Reg<15:0>
112
116'
Row Select
Error Control
Frame Delay Register Write Control
Frame Delay Data<15:0>
118'
Error Code <15:0>
15<15:0>
14<15:0>
13<15:0>
12<15:0>
11<15:0>
10<15:0>
9<15:0>
8<15:0>
7<15:0>
6<15:0>
5<15:0>
4<15:0>
3<15:0>
2<15:0>
1<15:0>
0<15:0>
114
FAR Register/Error Code Register <15:0>
FDR Register<15:0>

FIG. 7.

Input Stream Offset	Measurement Result from Frame Delay Bits				Corresponding Offset Bits			
	FD11	FD2	FD1	FD0	OFn2	OFn1	OFn0	DLEn
No clock period shift (Default)	1	0	0	0	0	0	0	0
+0.5 clock period shift	0	0	0	0	0	0	0	1
+1.0 clock period shift	1	0	0	1	0	0	1	0
+1.5 clock period shift	0	0	0	1	0	0	1	1
+2.0 clock period shift	1	0	1	0	0	1	0	0
+2.5 clock period shift	0	0	1	0	0	1	0	1
+3.0 clock period shift	1	0	1	1	0	1	1	0
+3.5 clock period shift	0	0	1	1	0	1	1	1
+4.0 clock period shift	1	1	0	0	1	0	0	0
+4.5 clock period shift	0	1	0	0	1	0	0	1
+5.0 clock period shift	1	1	0	1	1	0	1	0
+5.5 clock period shift	0	1	0	1	1	0	1	1
+6.0 clock period shift	1	1	1	0	1	1	0	0
+6.5 clock period shift	0	1	1	0	1	1	0	1
+7.0 clock period shift	1	1	1	1	1	1	1	0
+7.5 clock period shift (max)	0	1	1	1	1	1	1	1

FIG. 8.